

73 1/16/04

SHEET 1 OF 3

| INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449) | | | ATTY. DOCKET NO. 43876-158 | SERIAL NO. Continuation of Serial No. 10/646,787 | | |
|---|--|----------|--|--|----------|---|
| | | | APPLICANT HANSEN, et al. | | | |
| | | | FILING DATE January 16, 2004 | GROUP To be assigned | | |
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WDC99 864143-1.043876.0458

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| | | | APPLICANT HANSEN, et al. | | | | |
| (PTO-1449) | | | FILING DATE January 16, 2004 | GROUP To be assigned | | | |
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| EXAMINER'S INITIALS | PATENT NO. | DATE | COUNTRY | CLASS | SUBCLASS | Yes | No |
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WDC99 864144-1.043876.0158

| INFORMATION DISCLOSURE CITATION IN AN APPLICATION | | | ATTY. DOCKET NO. 43876-158 | SERIAL NO. Continuation of Serial No. 10/646,787 | | | |
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| | | | APPLICANT HANSEN, et al. | | | | |
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| EXAMINER'S INITIALS | PATENT NO. | DATE | COUNTRY | CLASS | SUBCLASS | Yes | No |
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[Handwritten signature] Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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SHEET 1 OF 1

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|--|----------|---|--------------------------------|--|--|---|
| | | | | APPLICANT Craig HANSEN et al | | |
| (PTO-1449) | | | | FILING DATE Jan. 16, 2004 | GROUP To be assigned | |
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| EXAMINER'S INITIALS | CITE NO. | Document Number Number-Kind Code (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
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| OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | |
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WDC99 866514-1.043876.0158



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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i> | | | | Application Number | 10/757,925 |
| Sheet | 1 | of | 10 | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| | | | | Attorney Docket Number | 43876-158 |

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| Examiner Signature | <i>[Signature]</i> | Date Considered | 4/11/08 |
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| INFORMATION DISCLOSURE STATEMENT BY APPLICANT | | | | Application Number | 10/757,925 |
| <i>(use as many sheets as necessary)</i> | | | | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 2 | of | 10 | Attorney Docket Number | 43876-158 |

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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | | | T ² |
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| Examiner Signature | <i>Very</i> | Dated Considered | 4/11/06 |
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| <p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p><i>(use as many sheets as necessary)</i></p> <p>Sheet 3 of 10</p> | | | | <p><i>Complete if Known</i></p> <table border="1"> <tr> <td>Application Number</td> <td>10/757,925</td> </tr> <tr> <td>Filing Date</td> <td>January 16, 2004</td> </tr> <tr> <td>First Named Inventor</td> <td>Craig C. HANSEN, et al.</td> </tr> <tr> <td>Group Art Unit</td> <td>2183</td> </tr> <tr> <td>Examiner Name</td> <td>CHAN, EDDIE P</td> </tr> <tr> <td>Attorney Docket Number</td> <td>43876-158</td> </tr> </table> | Application Number | 10/757,925 | Filing Date | January 16, 2004 | First Named Inventor | Craig C. HANSEN, et al. | Group Art Unit | 2183 | Examiner Name | CHAN, EDDIE P | Attorney Docket Number | 43876-158 |
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| Filing Date | January 16, 2004 | | | | | | | | | | | | | | | |
| First Named Inventor | Craig C. HANSEN, et al. | | | | | | | | | | | | | | | |
| Group Art Unit | 2183 | | | | | | | | | | | | | | | |
| Examiner Name | CHAN, EDDIE P | | | | | | | | | | | | | | | |
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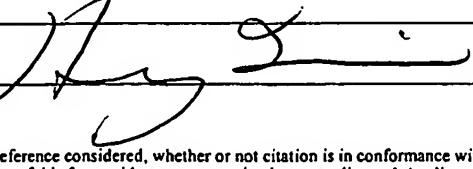
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| <i>HS</i> | BX | Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 - 351) | | | |
| <i>HS</i> | BY | Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 - 090) | | | |
| <i>HS</i> | BZ | Undy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 - 590) | | | |
| <i>HS</i> | CA | HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 - 141) | | | |
| <i>HS</i> | CB | PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 - 176) | | | |
| <i>HS</i> | CC | Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 - 776) | | | |
| <i>HS</i> | CD | Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 - 519) | | | |
| <i>HS</i> | CE | Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 - 751) | | | |
| <i>HS</i> | CF | Gipper, "Designing Systems for Flexibility, Functionality, and Performance with the 88110 Symmetric Superscalar Microprocessor," IEEE (1992) (51056DOC008758 - 763) | | | |
| <i>HS</i> | CG | Nikhil et al., "*T: A Multithreaded Massively Parallel Architecture," Computation Structures Group Memo 325-2, Laboratory for Computer Science, Massachusetts Institute of Technology (March 5, 1992) (51056DOC002464 - 476) | | | |
| <i>HS</i> | CH | Papadopoulos et al., "*T: Integrated Building Blocks for Parallel Computing," ACM, pp. 624-35 (1993) (51056DOC007278 - 289) | | | |
| <i>HS</i> | CI | Patterson, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip," Motorola Computer Group (Sept. 1992) (51056DOC069260 - 262) | | | |
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| <i>HS</i> | CK | M. Smotherman et al., "Instruction Scheduling for the Motorola 88110," IEEE, 1993 (51056DOC008784 - 789) | | | |
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| <i>HS</i> | CO | J. Maguire, "MC88110: Datpath," Northcon, 1992 (51056DOC010059 - 063) | | | |
| <i>HS</i> | CP | Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 - 646) | | | |
| <i>HS</i> | CQ | Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 - 661) | | | |
| <i>HS</i> | CR | Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 - 656) | | | |
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| <i>HS</i> | CT | Takahashi et al., "A 289 MFLOPS Single Chip Vector Processing Unit," The Institute of Electronics, Information, and Communication Engineers Technical Research Report, pp. 17-22 (May 28, 1992) (51056DOC009798 - 812) | | | |

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| Examiner Signature | <i>John S</i> | Dated Considered | 4/11/06 |
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| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | | | |
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | | | |
|  | CU | Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 - 194) | | | |
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| | CW | Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291) | | | |
| | CX | Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 - 034) | | | |
| | CY | Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 - 279) | | | |
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| | DA | Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895) | | | |
| | DB | The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 - 607) | | | |
| | DC | S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 - 918) | | | |
| | DD | Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758) | | | |
| | DE | Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618) | | | |
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| | DG | Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376) | | | |
| | DH | Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157) | | | |
| | DI | "Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390) | | | |
| | DJ | Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993) | | | |
| | DK | Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598) | | | |
| | DL | Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236) | | | |
| | DM | Saturn Overview (November 12, 1993) (51056DOC017111 - 157) | | | |
| | DN | Convex Notebook containing various "Machine Descriptions" (51056DOC016994 - 7510) | | | |
| | DO | "Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383) | | | |
| | DP | Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 - 443) | | | |
| DQ | Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 - 459) | | | | |
| DR | Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 - 5299) | | | | |
|  | DS | Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394) | | | |

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| Examiner Signature |  | Dated Considered | 4/11/06 |
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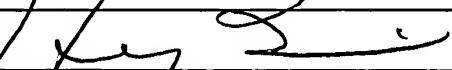
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| Sheet | 6 | of | 10 | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| | | | | Attorney Docket Number | 43876-158 |

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T ² |
|--------------------|-----------------------|---|----------------|
| CH | DT | Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042) | |
| | DU | AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392) | |
| | DV | Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 - 666) | |
| | DW | Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. 1, pp. 275-84 (April 17-20, 1989) (5156DOC070711 - 717) | |
| | DX | Grimes et al., "The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities," IEEE Computer Graphics & Applications, pp. 85-94 (July 1989) (5156DOC070701 - 710) | |
| | DY | Kohn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 - 094) | |
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| | EC | Margulies, "i860 Microprocessor Architecture," Intel Corporation (1990) (51056DOC066610 - 7265 and 5156DOC069971 - 7026) | |
| | ED | Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 - 700) | |
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| | EF | Rhodehamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 - 647) | |
| | EG | Perry, "Intel's Secret is Out," IEEE Spectrum, pp. 22-28 (April 1989) (5156DOC070648 - 654) | |
| | EH | Sit et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 - 101) | |
| | EI | i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 - 427) | |
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| | EK | N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982) | |
| | EL | N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551) | |
| | EM | N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509) | |
| | EN | N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441) | |
| | EO | N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851) | |
| | EP | N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 - 73027) | |
| | EQ | Hansen, "Architecture of a Broadband Mediaprocessor," IEEE COMPON 96 (February 25-29, 1996) (MU0013276 - 283 and 51057DOC001825 - 831) | |
| CH | ER | Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 - 630) | |

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| ES | | Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 - 958) | | | |
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| EU | | Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 - 040) | | | |
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| EW | | Donovan et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, pp. 51-61 (January 1995) (51056DOC059635 - 645) | | | |
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| EY | | Geist, "Cluster Computing: The Wave of the Future?," Oak Ridge National Laboratory, 84OR21400 (May 30, 1994) (51056DOC020924 - 929) | | | |
| EZ | | Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705) | | | |
| FA | | Gilioi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801) | | | |
| FB | | Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 - 673) | | | |
| FC | | Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 - 662) | | | |
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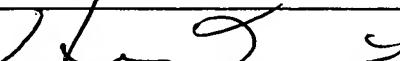
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| Examiner Signature | <i>Key D</i> | Dated Considered | 4/11/06 |
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| <p>Substitute for form 1449B/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p><i>(use as many sheets as necessary)</i></p> | | | | Complete if Known | |
| | | | | Application Number | 10/757,925 |
| | | | | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 8 | of | 10 | Attorney Docket Number | 43876-158 |

| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | | | |
|---|-----------------------|--|--|--|----------------|
| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | | | T ² |
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| Examiner Signature |  | Dated Considered | 4/11/08 |
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| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 9 | of | 10 | Attorney Docket Number | |
| 43876-158 | | | | | |

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| <i>JK</i> | GI | IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (S1056DOC019304 - 323) | | | |
| <i>JK</i> | | Original Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004 | | | |
| | GJ | Amended Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004 | | | |
| | GK | Expert Witness Report of Richard A. Killworth, Esq., <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005 | | | |
| | GL | Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005 | | | |
| | GM | Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-1; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005 | | | |
| | GN | Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005 | | | |
| | GO | Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005 | | | |
| | GP | Request for <i>Inter Partes</i> Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005 | | | |
| | GQ | Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division | | | |
| | GR | Deposition of Leslie Kohn on September 22, 2005; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division | | | |
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| | GV | The Wall Street Journal Article, "Intel Says Chip Demand May Slow", October 19, 2005 | | | |
| <i>JK</i> | GW | The New York Times Article, "Intel Settlement Revives A Fading Chip Designer", October 20, 2005 | | | |

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| Examiner Signature | <i>JK</i> | Dated Considered | <i>4/11/06</i> |
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| INFORMATION DISCLOSURE CITATION IN AN APPLICATION | | | | ATTY. DOCKET NO. 043876-0158 | SERIAL NO. 10/757,925 | |
|---|-------------|---|-----------------------------------|--|---|-------------|
| (PTO-1449) | | | | APPLICANT Craig HANSEN, et al. | | |
| FILING DATE January 16, 2004 | | | | GROUP 2183 | | |
| U.S. PATENT DOCUMENTS | | | | | | |
| EXAMINER'S INITIALS | CITE NO. | Document Number Number-Kind Codez (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear | |
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| KJ | | | | | | Yes |
| KJ | | | | | | No |
| OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | |
| KJ | CITE NO. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | | | | |
| KJ | C | MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005) | | | | |
| KJ | D | Intel Press Release, "Intel Announces Record Revenue of \$9.96 Billion," Santa Clara, CA, 10-18-2005 | | | | |
| EXAMINER <i>Dee S.</i> | | | DATE CONSIDERED <i>4/11/06</i> | | | |

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SHEET 1 OF 11

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APPLICATION

(PTO-1449)

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043876-0158

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APPLICANT
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| EXAMINER <i>Clay S.</i> | | DATE CONSIDERED <i>4/11/06</i> | |

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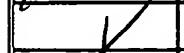
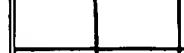
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| | L-129 | "IEEE Draft Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", 1995, pp.1-104, IEEE. | |
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| | L-137 | JOE HEINRICH, "MIPS R4000 Microprocessor User's Manual Second Edition"1994 MIPS Technologies, Inc. pp. 1-754. | |
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| | L-145 | Supplementary European Search Report dated March 18, 2005, corresponding to Application No. 96928129.4 | |
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